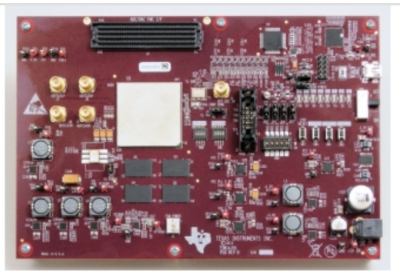
ADC Ti TSW14J56EVM



TSW14J56EVM Evaluation Module Top View

Short description : **The Texas Instruments TSW14J56 Evaluation Module** (EVM) is a next generation of pattern generator and data capture card used to evaluate performances of the new Texas Instruments (TI) JESD204B family of high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC).

Populated with an Arria V GZ device and using Altera's JESD204B IP solution, the TSW14J56 can be dynamically configurable to support all lanes speeds from 600Mbps to 10.3125Gbps, from 1 to 8 lanes, 1 to 16 converters, and 1 to 4 octets per frame.

Together with the accompanying High Speed Data Converter Pro Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from ADC EVM's and generates and sends desired test patterns to DAC EVM's. **Features**

- Quickly evaluate JESD204B DAC and ADC performance using TI High Speed Data Converter Pro software
- Direct connection to all TI JESD204B High Speed Data Converter EVM's using an FMC standard connector
- Quarter rate DDR3 controllers supporting up to 800MHz DDR3 operation
- JESD RX and TX IP cores with 10 routed transceiver channels
- Many available general purpose IO's (status signals, SPI interface, etc.) between the FPGA and the FMC connector
- SPI/JTAG reconfigurable JESD core parameters: L,M,K,F,HD,S etc.
- Support for SUBCLASS 0 and 1 operation
- Dynamically reconfigurable transceiver data rate using HSDC Pro software.
- Operating range from 0.611Gbps to 10.3125Gbps
- For support for a 12.5Gbps JESD204B pattern generator solution :
https://focus.ti.com/general/docs/event/accesseventaction.tsp?actionId=1426
- 8Gb x64 DDR3 SDRAM (split into two independent x32 4Gb SDRAMs, total of 256M 16-bit samples each)

Localisation : Maxime Drouguet

Personne(s) ressource(s) : Maxime Drouguet,

Site Web : www.uclouvain.be/welcome
Contact : info-welcome@uclouvain.be