LELEC2570 Synthesis of digital integrated circuits

1q

5.0 credits

2013-2014

UCL

Université catholique de Louvain

30.0 h + 30.0 h

Teacher(s) :	Legat Jean-Didier ; Bol David ;
Language :	Anglais
Place of the course	Louvain-la-Neuve
Inline resources:	Moodle
	> http://moodleucl.uclouvain.be/enrol/index.php?id=3
Prerequisites :	 The basic formation in digital electronic circuits is compulsory: LELEC1530 and LELEC2531.
	A course in embedded system design is an advantage: LINGI2315.
Main themes :	The exponential increase in computing performances of digital integrated circuits (ICs) fundamentally modified our everyday's life in numerous domains (consumer, business, medical, industrial). Nowadays these circuits feature several millions of transistors, which leads to a high design complexity. Therefore, digital circuit design requires the use of methodologies and computer-aided design (CAD) tools within a systematic design flow. In this course, we will study the automatic synthesis of very-large scale integration (VLSI) digital ICs (microprocessors, ASICs) using a top-down synthesis flow from system design to its translation in a logic-gate netlist to its physical implementation on a silicon die (layout).
Aims :	a. Contribution of the activity to the learning outcomes of the program AA1 Knowledge base : electronic concepts (AA1.1), simulation and CAD tools (AA1.2) AA2 Engineering skills : analysis, design and implementation of a digital integrated circuit, AA3 R& mp;D skills : find appropriate references on the existing solutions in the field of the course's project (AA3.1), AA5 Communication skills : efficient written communication respecting the contextual specificities.(AA5.5).
	 b. Learning outcomes After this course, the electrical engineers in circuit and systems should be able to: produce the layout of a digital IC in a modern CMOS technology starting from a behavorial description and using industrial-level
	CAD tools, discuss the trade-offs linked to the synthesis of digital ICs between silicon area, computing performance, power consumption, flexibility and robustness,
	 setup a strategy for verifying the obtained results using SystemVerilog simulation,
	 rapidly evaluate the efficiency of high-level architectural solutions using SystemC simulation,
	 communicate clearly and efficiently technical results in a circuit design report. The contribution of this Teaching Unit to the development and command of the skills and learning outcomes of the programme(s) can be accessed at the end of this sheet, in the section entitled "Programmes/courses offering this Teaching Unit".
Evaluation methods :	The individual evaluation is based on 12 short assignments during the semester and on the final project, which consists in the delivery of a report at the end of the semester and an oral discussion of the project results during the exam session.
Teaching methods :	The course is organized as follows.
	14 lectures and/or specific seminars given by experts from the industrial world regarding the design of digital ICs. They will be broadly illustrated by recent digital IC examples from both the industrial and research worlds.
	A central individual project on the full design of a digital IC with weekly milestones linked to the steps of the synthesis flow. This self-learning project will be based on industrial CAD tools. The interaction between the students, the teachers and assistants will be encouraged by the use of a discussion forum on Moodle platform.
Content :	 Behavioral modeling of digital systems in SystemC

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	Robust HDL coding in Verilog
	 Logic synthesis of digital circuits
	 Place and route of digital circuits
	 Timing and library optimization
	Verification of digital systems in SystemVerilog
Bibliography :	Supports
	Slides of the lectures on Moodle
	 Reference text book: Digital VLSI Chip Design with Cadence and Synopsys CAD Tools by Erik Brunvand
	Forum on Moodle
	 Technical documentation on Moodle
Cycle and year of study :	 Master [120] in Electro-mechanical Engineering Master [120] in Electrical Engineering
Faculty or entity in charge:	ELEC