LELEC2570

2012-2013

Synthesis of digital integrated circuits

5.0 credits	30.0 h + 30.0 h	1q

Teacher(s) :	Legat Jean-Didier ;
Language :	Français
Place of the course	Louvain-la-Neuve
Prerequisites :	LELEC 2531 : Design and Architecture of digital electronic systems
Main themes :	Identical to description
Aims :	At the end of this course, the students will be able to -- Design, simulate and synthesize a digital specific integrated circuit (ASIC) -- Be able to use Cadence and Synopsys -- Design and simulate basic cells -- Incorporate these basic cells in the design of the ASIC -- Optimize the synthesis of the ASIC *The contribution of this Teaching Unit to the development and command of the skills and learning outcomes of the programme(s) can be accessed at the end of this sheet, in the section entitled "Programmes/courses offering this Teaching Unit".*
Evaluation methods :	The evaluation is based on the work during the semester and the final project
Teaching methods :	-- Learning is based on courses accompanied by seminars, homework and a project. -- Each student will design and simulate an ASIC in the project
Content :	-- Logic synthesis -- The optimization software -- Optimizing hardware -- Placement and routing -- The optimization time -- Full custom design of basic cells -- The layout and integration of basic cells -- Synthesis and optimization of the final ASIC
Bibliography :	Digital VLSI Chip Design with Cadence and Synopsys CAD Tools by Erk Brunvand
Cycle and year of study :	> Master [120] in Electrical Engineering > Master [120] in Electro-mechanical Engineering
Faculty or entity in charge:	ELEC